DXC-2

T1/E1 Converter and Timeslot Cross-connect

FEATURES

- Converts between T1 and E1 data and signaling
- Configurable A-law/μ-law and signaling conversion, or transparent conversion at 64 kbps timeslot level
- Soft-selectable to comply with CCITT Rec. G.802, Annex 2
- Optionally available with built-in CSU (T1) and LTU (E1)
- Controlled slip for buffer overflow/underflow
- Monitoring and control from terminal or from front panel
- Loopback capabilities
- E1/E1 or T1/T1 timeslot cross-connect with optional frame conversion
- Compact, easy to install

DESCRIPTION

The DXC-2, T1/E1 Converter and Timeslot Cross-connect enables conversion between one T1 signal and one E1 signal (24 timeslots).

The signal can be optionally provided with a built-in CSU for T1 and LTU for E1 (see Ordering).

The DXC-2 can also be ordered with two ports of the same type (two E1 or two T1). This allows the reshuffling of timeslots or the modifying of framing patterns; for example, D4 to ESF for a T1 product, or G.704 without CRC-4 to G.704 with CRC-4 for an E1 product.

The DXC-2 utilizes a user-programmable connection table for connecting any incoming 64 kbps timeslot to any outgoing 64 kbps timeslot. Programming can be performed during system operation, without disruption to service.

The T1 to E1 can be set to comply with CCITT G.802, Annex 2 (soft-selectable). This enables the location of the T1 F-bit to be specified in the E1 data stream.

For conversion between T1 and E1 trunks, the DXC-2 can perform the required A-law/μ-law and signaling conversion, in compliance with T1 and E1 (CEPT) standards.

Maintenance capabilities include local and remote loopback. When operating in ESF format, T1 link statistics are stored in memory in compliance with both the ANSI and AT&T standards. When operating in CRC-4 format, E1 link statistics are stored in memory in compliance with CCITT G.706.

Selectable timing options cover all timing possibilities for the T1/E1 interface. These include internal clock and loopback timing, for either the T1 or E1 interface.

The T1 interface complies with AT&T TR-62411 and ANSI T1.403 requirements, and supports both D4 or ESF framing formats and AMI line code. Zero suppression is selectable for transparent, B7ZS or B8ZS.

The E1 interface complies with CCITT Rec. G.703, G.704, G.732 and G.823, and supports both 2 and 16 frames per multiframe without CRC-4, and framing with CRC-4. Line code is HDB3.

Setup, control, status, alarms and diagnostic information can be monitored and controlled via the front panel LCD display or via an ASCII terminal.

The DXC-2 is a compact 1U high desk-top unit, with optional rack-mount hardware for mounting in a 19" rack (see Ordering).

SPECIFICATIONS

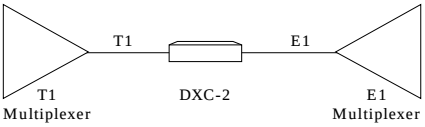
T1 Interface

Compliance:
AT&T TR-62411, ANSI T1.403
CCITT Rec. G.703, G.704
Framing: D4, ESF
Data Rate: 1.544 Mbps
Line Code: AMI
Impedance: 100 Ω, balanced
Zero suppression:
Transparent, B7ZS, B8ZS
Signal Levels:
Receive:
0 to -40 dB with CSU
0 to -10 dB without CSU
Transmit:
0 dB, -7.5 dB, -15 dB with CSU
3V, ±10% soft-adjustable to be measured at 0 to 655 ft without CSU
Jitter Performance:
As per AT&T TR-62411
Connector: 15-pin D-type, female

E1 Interface

Compliance:
Rec. G.703, G.704, G.732
Framing:
With CRC-4: TS0 MF, CAS
With CRC-4: TS0 MF, CCS
Without CRC-4, CAS: TS16 MF
Without CRC-4, CCS: no MF
Data Rate: 2.048 Mbps
Line Code: HDB3
Impedance: 120 Ω, balanced
75 Ω, unbalanced
Signal Level:
Receive:
0 to -40 dB with LTU
0 to -10 dB without LTU
Transmit:
Balanced: ±3V, ±10%
Unbalanced: ±2.37V, ±10%
Jitter Performance:
As per CCITT G.823
Connectors:
15-pin D-type, female, for balanced
Two BNC coaxial, for unbalanced

APPLICATION



GENERAL

Timeslot Mapping

Any timeslot to any timeslot with/without A-law/μ-law and signaling conversion per timeslot

Timing

TCLK-A, TCLK-B, System Clock
Source:
Internal timing (±32 ppm)
Receive clock link A (LBT-A)
Receive clock link B (LBT-B)

Elastic Buffer

Buffer length: ± 1 frame
Underflow: 1 frame repeated
Overflow: 1 frame skipped
(No frame sync loss for buffer overflow or underflow)
Data delay: up to 375 msec

Unused Timeslot Code

T1 interface: user defined
E1 interface: user defined

Diagnostics

Local T1 or E1 loopback
Remote T1 or E1 loopback
Code activated network loopback per ANSI T1.403

Statistics

T1 ESF performance monitor:
ANSI T1.403 full support
AT&T 54016 local support
Transparent FDL between two T1 ports
E1 CRC-4 performance monitor:
Per CCITT G.706

Alarm Response (both directions)

Received impairment on link A:
Loss of signal/frame, yellow alarm
Transmit response on link A (in loss of signal/frame): yellow alarm
Transmit response on link B (on connected TS):
DS-0 OOS pattern,
OOS A, B signaling

Front Panel Controls

LCD: 2 rows x 16 characters
Push buttons: cursor, scroll, enter

Supervisory Port

Interface: V.24/RS-232, async
Connector: 9-pin D type, female
Data Rate: 300-9600 bps, autobaud

Indicators

Local sync loss: link A, link B
Remote sync loss: link A, link B
Test

Physical

Height:	4.4	cm /	1.7	in (1U)
Width:	21.6	cm /	8.4	in
Depth:	24.0	cm /	9.5	in
Weight:	1.4	kg /	3.1	lb

Power

115/230 VAC (±10%)
47-63 Hz,
-48 VDC (±10%), 15 watts

Environment

Temperature: 0-50°C/32-122°F
Humidity: Up to 90%, non-condensing

ORDERING

DXC-2/*/&/#
T1/E1 Converter and Timeslot Machine

* Specify:
115 for 115 VAC supply
230 for 230 VAC supply
48 for -48 VDC supply

& Specify:
2T1 for dual T1 ports
2E1 for dual E1 ports
(Default is one T1 and one E1 port)

Specify:
C1 for CSU/LTU in port 1
C2 for CSU/LTU in port 2
(Default is without CSU/LTU)

Specifications are subject to change without prior notification

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